

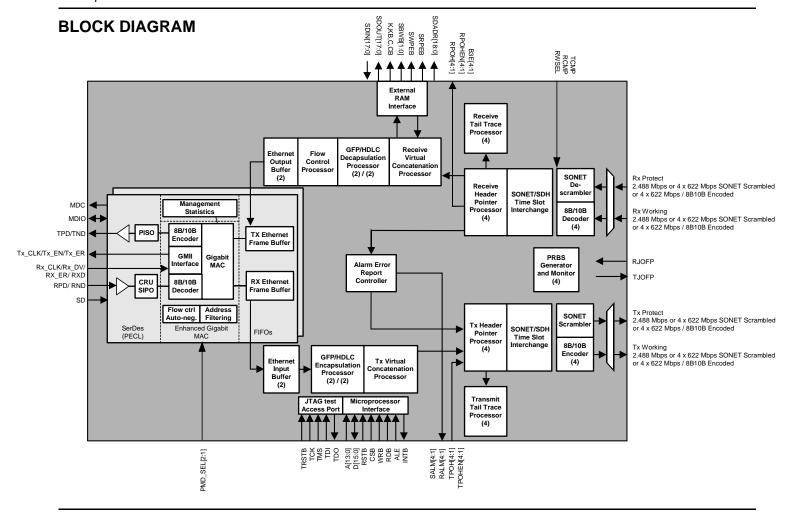
Two Channel Gigabit Ethernet to SONET Mapping Device

FEATURES

- Maps each of two channels of Gigabit Ethernet using the Generic Framing Procedure (GFP) point-to-point Ethernet over SONET (EoS) encapsulation protocol, or HDLC delineation into a standards-based virtual concatenation stream comprising 1 to 8 STS-3c/VC-4 or 1 to 24 STS-1/VC-3 channels.
- Alternatively maps one Gigabit
 Ethernet channel into an STS-48c
 channel or independently maps each
 Gigabit Ethernet channel into either an
 STS-12c or an STS-24c payload.
- Supports full-rate data transfer and over-subscribed data transfer down to STS-1/VC-3 granularity for Gigabit Ethernet data transfer over SONET/SDH. Ethernet back pressure prevents packet loss when the SONET channel is configured to be less than 1 Gbps.

- Supports interfacing to any full duplex IEEE 802.3 Gigabit Ethernet connection.
- Preserves Ethernet frame, discards IPG, preamble and SFD during mapping, and restores them during demapping.
- Incorporates dual SerDes, compliant with the IEEE 802.3 PMA physical layer specification.
- Supports maximum Ethernet frame size of 9,600 bytes.
- Supports an ingress Ethernet buffer of 92.8 Kbytes and an egress Ethernet buffer of 28.8 Kbytes.
- Supports serial differential or parallel GMII Ethernet side transmit and receive Gigabit Ethernet signals.
- Supports IEEE 802.3 flow control, auto-negotiation, and management statistics on Gigabit Ethernet interfaces.

- Provides working and protect 4 x 777.6 MHz LVDS Serial TelecomBus, 4 x 622 Mbps LVDS SONET Serial, or 2.488 Gbps LVDS SONET Serial interfaces.
- Supports an on-chip differential delay buffer of one STS-48/STM-16 frame for virtual concatenation.
- Optional off-chip Quad Data Rate (QDR) SRAM supports differential delay of STS-48/STM-16 frames up to 50 ms.
- Performs SONET/SDH path termination, including the processing of H4, C2 and J1 bytes for virtual concatenation.
- Performs alignment of virtual concatenation constituent SONET/SDH channels in the receive direction.
- Performs splitting of user data into multiple constituent SONET/SDH



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- channels and generates required SONET/SDH path overhead bytes in the transmit direction.
- Supports the assignment of SONET/SDH channels using an STS-1 Time Slot Interchange to arbitrary SONET timeslots on working and protect interfaces.
- Offers per-channel Ethernet side and SONET system side loopback for system level diagnostic capability.
- Provides on-chip data recovery and clock synthesis for Gigabit Ethernet and SONET Serial system interfaces.

GENERAL

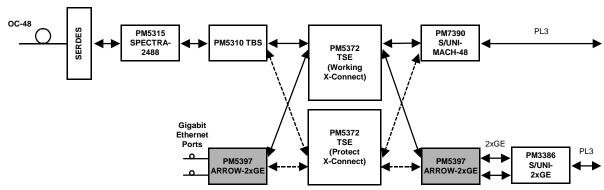
- Provides a general-purpose 16-bit microprocessor interface for configuration, management and statistics gathering.
- Provides a standard 5 signals P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 1.8 V core with 5.0 V tolerant 3.3 V TTL compatible I/O.
- Industrial temperature range (-40 °C to +85 °C).
- 896-pin FCBGA package.

APPLICATIONS

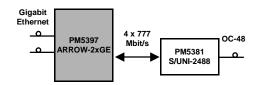
- High density Gigabit Ethernet to SONET port cards, mapping multiple Gigabit Ethernet channels into OC-48 or OC-192 streams.
- Gigabit Ethernet port cards for Multi-Service Provisioning Platforms.
- Non-blocking 128-512 port singlestage fabric Gigabit Ethernet Cross Connect.

TYPICAL APPLICATIONS

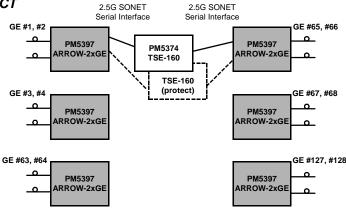
GIGABIT ETHERNET PORT CARD FOR MULTI-SERVICE PROVISIONING PLATFORM



GIGABIT ETHERNET TO SONET OC-48 PORT CARD



128 PORT GE CROSS CONNECT



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